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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,533	02/11/2002	Wayne W. Ballantyne	CS10721	6678

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EXAMINER	
PATEL, NIMESH G	
ART UNIT	**PAPER NUMBER**
2112	2

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,533	BALLANTYNE ET AL.	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,15 and 17* is/are rejected.

7)☒ Claim(s) *13 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5, 7, 8, 11-12 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 5 recites the limitation "the second main control unit" in lines 1 and 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 7 recites the limitation "the shift registers" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 8 recites the limitation "the second main control unit" in lines 1-3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 11 recites the limitation "the second main control unit" in lines 1 and 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 12 recites the limitation "the second main control unit" in lines 3-5 of the claim. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 17 recites the limitation "a common format." It is not clear as to what a common format is since it is not defined.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-6, 9-11, and 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Ma et al.('880), hereinafter referred to as Ma.

11. Regarding claim 1, Ma discloses an apparatus to allow dual master control of a slave peripheral unit, comprising: a first and a second master control unit(Figure 1, 120, 122; The components are masters in respect to the shared I/O port), each master control unit able to provide control bits(Transactions require control bits); a slave peripheral unit(I/O port) operable by a shared subset of the control bits from the master control units(Column 4, Lines 13-16); a slave peripheral interface coupled between the master control units and the slave peripheral unit(Figure 1, 100), the interface includes a data communication bus(Figure 2, 500, 502) for carrying the control bits; and a logic configuration block coupled to the communication bus, the logic configuration block controls access of the shared subset of control bits to the slave peripheral unit, the block configurable by a set of configuration bits accessible by only a first master control unit(Column 4, Lines 1-8).

12. Regarding claim 2, Ma discloses an apparatus, wherein the configuration bits set logic configuration bits in the logic configuration block, the logic configuration bits defining the control of the common subset of shared control bits by the master control units(Column 4, Lines 1-8).

13. Regarding claim 3, Ma discloses an apparatus, wherein the configuration bits set a logic operation in the logic configuration block, the logic operation operates on the shared control bits from the master control units to define a combined output set of control bits to control the peripheral(Column 4, Lines 1-8).

14. Regarding claim 4, Ma discloses an apparatus, wherein the slave peripheral unit includes respective first and second input registers coupled to the first and second master control units through the communication bus(Figure 2, 506-510), the input registers being coupled to provide the shared control bits from the master control units to the logic configuration block, and wherein the slave peripheral unit includes a configuration register(Figure 2, 504) accessible to the first master control unit and coupled to provide configuration bits to the logic configuration block(Column 4, Lines 13-23).

15. Regarding claim 5, Ma discloses an apparatus, wherein the second main control unit is operable to read the configuration register to confirm accessibility of the slave peripheral unit by the second main control unit(Column 4, Lines 54-55).

16. Regarding claim 6, Ma discloses an apparatus, wherein the slave peripheral unit includes an output to output the logical combination of the shared control bits of the master control units from the logic configuration block(Figure 2, 130).

17. Regarding claim 9, Ma discloses an apparatus to allow dual master control of a slave peripheral unit, comprising: a first and a second master control unit(Figure 1, 120, 122; The components are masters in respect to the shared I/O port), each master control unit able to provide control bits(Transactions require control bits); a slave peripheral unit(I/O port) operable by a shared subset of the control bits from the master control units(Column 4, Lines 13-16), the slave peripheral unit includes respective first and second input registers(Figure 2, 506-510) that receive the control bits from master control units and a configuration register(Figure 2, 504) accessible by the first master control unit; a slave peripheral interface(Figure 1, 100) including a data communication bus(Figure 2, 500, 502) coupled between the control units and the respective input registers of the slave peripheral unit, the communication bus for carrying the control bits; and a logic configuration block coupled to the input registers and the configuration

register, the logic configuration block controls access of the shared subset of control bits to the slave peripheral unit, the block configurable by a set of configuration bits from the configuration register(Column 4, Lines 1-8).

18. Regarding claim 10, Ma discloses an apparatus, wherein the configuration bits set a logic operation in the logic configuration block, the logic operation operates on the shared control bits from the master control units to define a combined output set of control bits to control the peripheral(Column 4, Lines 1-8).

19. Regarding claim 11, Ma discloses an apparatus, wherein the second main control unit is operable to read the configuration register to confirm accessibility of the slave peripheral unit by the second main control unit(Column 4, Lines 54-55).

20. Regarding claim 14, Ma discloses a method of providing dual master control of a slave peripheral unit, the method comprising the steps of: providing a first set of control bits and a set of logic configuration bits from a first master control unit(Column 4, Lines 1-8), and providing a second set of control bits from a second master control unit(Transaction require control bits); configuring a logic operation in a combinational logic block with the set of logic configuration bits; performing the logical operation on the first and second set of control bits to provide a resultant set of control bits; and applying the resultant control bits to a slave peripheral unit(Column 4, Lines 1-8).

21. Regarding claim 15, Ma discloses a method, further comprising the step of reading the configuration bits by the second master unit to confirm accessibility of the slave peripheral unit(Column 4, Lines 54-55).

Allowable Subject Matter

22. Claims 13 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP *NP*
June 9, 2004

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100